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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,449	11/02/2001	Lawrence J. Madar III	42112/CAG/B600	3578

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CHRISTIE, PARKER & HALE, LLP
PO BOX 7068
PASADENA, CA 91109-7068

EXAMINER	
ANDERSON, MATTHEW D	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 05/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,449	MADAR ET AL.	
	Examiner	Art Unit	
	Matthew D. Anderson	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-87* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-18,21-29,40-47,55-61,63-66,68,69 and 80-82* is/are rejected.

7)☒ Claim(s) *2,19,20,30-39,48-54,62,67,70-79 and 83-87* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/9/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 48, 59-61, and 79 are objected to because of the following informalities. Appropriate correction is required.

2. Should "base" instead read "based" in line 10 of claim 48?

3. Should "driving the one or more requests" in claims 59-61 instead read "driving the first set of one or more requests" to more clearly show the antecedent basis of claim 55?

4. Claim 79 appears to be mistakenly labeled as independent upon later claim 80. Should claim 79 instead be dependent upon claim 78? Also, no third clock is previously mentioned. Should the fourth clock in claim 79 instead be a third clock?

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3, 5-8, 10-12, 18, 21-29, 40-45, 47, 55-61, 63-69, and 81-82 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al. (US Patent # 5,440,713).

7. With respect to claim 1, Lin et al. disclose a memory divided into a plurality of memory blocks, one or more of the memory blocks configured to receive a plurality of requests; and a

memory access circuit configured to provide one of the plurality of requests to one of the plurality of memory blocks in a clock cycle, as taught in the abstract and figure 2.

8. With respect to claim 2, Lin et al. disclose wherein each request of the plurality of requests is provided to each of the plurality of memory blocks.

9. With respect to claim 3, Lin et al. disclose wherein the memory access circuit is configured to stall other requests for the memory block during the clock cycle, as taught by the halt signal being set during the arbitration cycle in column 5, liens 9+.

10. With respect to claim 4, Lin et al. disclose a local memory, wherein the local memory is configured to store an unsatisfied request.

11. With respect to claims 5 and 10, Lin et al. disclose wherein the plurality of requests comprises a plurality of new requests, as taught in the abstract.

12. With respect to claims 6 and 11, Lin et al. disclose wherein the plurality of requests comprises a plurality of previously unsatisfied requests, as taught in the abstract.

13. With respect to claims 7 and 12, Lin et al. disclose wherein the plurality of requests comprises one or more new requests and one or more previously unsatisfied requests, as taught in the abstract.

14. With respect to claim 8, Lin et al. disclose:

a memory divided into a plurality of memory blocks; and a plurality of memory block management circuits, each of the plurality of memory blocks associated with one of the memory block management circuits, as taught in the abstract and figure 2;

wherein each memory block management circuit is configured to: receive one or more requests from one or more requesters for one or more of the plurality of memory blocks, as taught in the abstract;

and on a single clock cycle (arbitration cycle in column 5, lines 9+), determine whether one of the memory blocks is requested by one or more of the requesters, determine which request is provided to said one of the memory blocks if one of the memory blocks is requested by one or more of the requesters, and provide the determined request to said one of the memory blocks, as taught in the abstract.

15. With respect to claim 18, Lin et al. disclose wherein the determination of which request is provided to said one of the memory blocks is based on an arbitration, as taught in the abstract.

16. With respect to claim 21, Lin et al. disclose wherein the determination of which request is provided to said one of the memory blocks is based on programmable criteria, as taught in column 3, lines 3-5, when discussing giving priority to requests with the same row address as the previous request.

17. With respect to claim 22, Lin et al. disclose wherein the determination of which request is provided to said one of the memory blocks is based on a dynamic response to usage patterns, as taught in column 3, lines 3-5, when discussing giving priority to requests with the same row address as the previous request.

18. With respect to claim 23, Lin et al. disclose wherein the one or more of the requests includes a priority request, as taught in column 3, lines 3-5, when discussing giving priority to requests with the same row address as the previous request.

19. With respect to claim 24, Lin et al. disclose wherein the priority request is determined to access said one of the memory blocks before other requests, as taught in column 3, lines 3-5, when discussing giving priority to requests with the same row address as the previous request.

20. With respect to claim 25, Lin et al. disclose the priority request comprising an input/output request, as taught in column 1, line 10.

21. With respect to claim 26, Lin et al. disclose wherein the memory block management circuit further comprises: an interface configured to receive the one or more requests from the one or more requesters; an arbiter coupled to the interface, the arbiter configured to: consider the one or more requests, determine whether one of the plurality of memory blocks is requested, and determine which of the one or more requests is provided to said one of the memory blocks; and a selection circuit configured to route the determined request from the interface to said one of the memory blocks based on the arbiter determinations, as taught in the abstract and figure 2.

22. With respect to claim 27, Lin et al. disclose the selection circuit comprising a multiplexer, as shown in figures 2-3.

23. With respect to claim 28, Lin et al. disclose wherein the arbiter determinations are based on request identification data, as taught in column 3, lines 3-5, when discussing giving priority to requests with the same row address.

24. With respect to claim 29, Lin et al. disclose wherein the determined request data is routed to an input of the selection circuit, as shown in figures 2-3.

25. With respect to claim 40, Lin et al. disclose a bus configured to transmit the one or more requests to the plurality of memory blocks through respective memory block management circuits, as shown in figure 2.

26. With respect to claim 41, Lin et al. disclose the bus comprises a stall bus, the memory block management circuits being configured to: receive a stall signal from the stall bus and prevent the unsatisfied requesters from accessing said one of the memory blocks based on the stall signal, as taught in figure 3 and column 4, lines 23-25.

27. With respect to claim 42, Lin et al. disclose the bus comprising a request bus configured to carry request data from the one or more requesters to the memory management circuits corresponding to a requested memory block, as shown in figure 2.

28. With respect to claim 43, Lin et al. disclose the bus comprising a memory bus configured to carry data retrieved from the requested memory block to a storage element associated with the request, as shown in figure 2.

29. With respect to claim 44, Lin et al. disclose a plurality of request management circuits, wherein each of the one or more requesters is associated with one of the plurality of request management circuits, and each of the plurality of request management circuits are configured to interface between a memory bus carrying data retrieved from said one of the memory blocks and the one or more requesters, as shown in figure 2.

30. With respect to claim 45, Lin et al. disclose a control circuit configured to receive:

a stall signal generated by the memory management circuit of the requested memory block, as taught in column 4, lines 23-25;

and an address signal, read from the one or more requests, identifying the requested memory block, as taught in column 4, line 40,

the control circuit being configured to generate a selection signal based on the stall signal and the address signal, as taught in column 4, line 30 – column 5, line 20;

and a multiplexer configured to receive the selection signal and select bus lines carrying data requested by the one or more requesters, as shown in figure 3.

31. With respect to claim 47, Lin et al. disclose the control circuit further comprising a delay system configured to synchronize the selection signal to pass the requested data through the multiplexer, as taught in column 6, lines 45-47.

32. With respect to claim 55, Lin et al. disclose a method of processing requests for memory, comprising: during a first clock (column 5, lines 9+), driving a first set of one or more requests from one or more requesters onto a request bus, performing a first determination whether one of a plurality of memory blocks is requested by the one or more requests, and if two or more requesters issue requests for one of the plurality of memory blocks, performing a second determination of which request of the two or more requests is provided to said one of the memory blocks, as taught in the abstract.

33. With respect to claim 56, Lin et al. disclose matching the one or more requests to the plurality of memory blocks by interleaving, as taught in the abstract.

34. With respect to claim 57, Lin et al. disclose that if one requester requests one of the plurality of memory blocks, further comprising providing the request to the requested memory block during the first clock, as taught in column 5, lines 9+.

35. With respect to claim 58, Lin et al. disclose that if two or more requests request one of the plurality of memory blocks, further comprising providing one of the two or more requests to the requested memory block based on the first and second determinations, as taught in the abstract.

36. With respect to claim 59, Lin et al. disclose wherein driving the one or more requests further comprises driving a new request onto the request bus, as taught in the abstract.

37. With respect to claim 60, Lin et al. disclose wherein driving the one or more requests further comprises driving a previously unsatisfied request onto the request bus, as taught in the abstract.

38. With respect to claim 61, Lin et al. disclose wherein driving the one or more requests further comprises driving a new request and a previously unsatisfied request onto the request bus, as taught in the abstract.

39. With respect to claim 63, Lin et al. disclose the second determination being based on an arbitration, as taught in the abstract.

40. With respect to claim 64, Lin et al. disclose the second determination being based on prioritizing one request relative to other requests, as taught in column 3, lines 3-5, when discussing giving priority to requests with the same row address as the previous request.

41. With respect to claim 65, Lin et al. disclose granting priority to an input/output request, as taught in column 1, line 10.

42. With respect to claim 66, Lin et al. disclose granting priority to a previously unsatisfied request, as taught in column 2, line 68.

43. With respect to claim 68, Lin et al. disclose the second determination being based on programmable criteria, as taught in column 3, lines 3-5, when discussing giving priority to requests with the same row address as the previous request.

44. With respect to claim 69, Lin et al. disclose the second determination being based on a dynamic response to usage patterns, as taught in column 3, lines 3-5, when discussing giving priority to requests with the same row address as the previous request.

45. With respect to claim 81, Lin et al. disclose wherein the one or more requests are issued from a processor, as taught in column 1, line 10.

46. With respect to claim 82, Lin et al. disclose wherein the one or more requests are issued from an input/output device, as taught in column 1, line 10.

Claim Rejections - 35 USC § 103

47. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

48. Claims 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. and Madar, III et al. (US Patent Publication # 2002/0056032).

49. With respect to claims 4 and 9, Lin et al. teach all other limitations, as discussed above, but fail to specifically disclose a local memory is configured to store an unsatisfied request that is not provided to said one of the memory blocks during the single clock cycle. Madar, III et al. though teach in paragraph 79 of a queue latch that stores previously stalled requests.

50. It would have been obvious to one of ordinary skill in the art, having the teachings of Lin *et al.* and Madar, III *et al.* before him at the time the invention was made, to modify the

arbitration system taught by Lin *et al.*, to include storage for stalled requests, as with the arbitration system of Madar, III *et al.*, in order ensure completion of any unsatisfied requests, as taught by Madar, III *et al.*.

51. Claims 13-17, 46, and 80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al.

52. With respect to claim 13, the difference between Lin *et al.* and the claims is the claims recite the memory being a single port memory. However, the specific use of a single port memory does not have a disclosed purpose nor are disclosed to overcome any deficiencies in the prior art. Accordingly, it would have been an obvious matter to one skilled in the art to utilize a single port memory instead of the memory of Lin *et al.* in order to reduce chip size, or any number of other desired engineering specifications.

53. With respect to claim 14, the difference between Lin *et al.* and the claims is the claims recite the memory being a SRAM memory. However, the specific use of a SRAM memory does not have a disclosed purpose nor are disclosed to overcome any deficiencies in the prior art. Accordingly, it would have been an obvious matter to one skilled in the art to utilize a SRAM memory instead of the DRAM memory of Lin *et al.* in order to not require a periodic refresh to retain data.

54. With respect to claim 15, the difference between Lin *et al.* and the claims is the claims recite the number of requests being less than the number of blocks. Accordingly, it would have been an obvious matter to one skilled in the art that upon initialization of the system (i.e., when

there are no requests) that the number of blocks in Lin et al. would exceed the number of requests for said blocks. Such would help to minimize stalls in the system.

55. With respect to claims 16 and 17, the difference between Lin *et al.* and the claims is the claims recite the number of requests being equal to or greater than the number of memory blocks. Although Lin et al. discloses a single request for a particular block and multiple requests for that particular block, there is not specific teaching of the total number of multiple request equaling or exceeding the total number of block. However, it would have been an obvious matter to one skilled in the art that a routine experimentation in the number of memory blocks in Lin et al. would easily cause the total number of blocks to be equal or less than that of the number of requests for a single block. Such would the limit the size and cost of the memory.

56. With respect to claim 46, the difference between Lin *et al.* and the claims is the claims recite the address signal comprising a binary number identifying a request memory block Although Lin et al. discloses a an address for the request for a particular block, there is not specific teaching of said address being a binary address. Lin et al. though disclose numerous other signals having a logical one or zero indicating binary computation. Accordingly, it would have been an obvious matter to one skilled in the art that the address signal would also be in binary format in order to optimize processing.

57. With respect to claim 80, the difference between Lin *et al.* and the claims is the claims recite the request being from a DMA device. However, the specific use of a DMA device does not have a disclosed purpose nor are disclosed to overcome any deficiencies in the prior art. Accordingly, it would have been an obvious matter to one skilled in the art to utilize a DMA device in the system of Lin *et al.* in order to transfer data without CPU intervention.

Allowable Subject Matter

58. Claims 2, 19-20, 30-39, 48-54, 62, 67, 70-79, and 83-87 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

59. The prior art does not teach or suggest the combination of claim elements specifically including at least the following:

[Claim 2]: wherein each request of the plurality of requests is provided to each of the plurality of memory blocks.

[Claim 19]: wherein the determination of which request is provided to said one of the memory blocks is based on a duration a request is unsatisfied.

[Claims 20 & 67]: wherein the determination of which request is provided to said one of the memory blocks is based on user-defined criteria.

[Claim 48]: the delay system comprising: a first delay circuit configured to receive the stall signal; a second delay circuit configured to receive the address signal; a third delay circuit configured to provide the address signal to said multiplexer; and a delay multiplexer configured to select one of two or more inputs base on an output of the first delay circuit, the inputs to the delay multiplexer comprising: an output of the second delay circuit, and an output of the third delay circuit.

[Claim 53]: wherein a request to write data to one of the plurality of memory blocks is completed in at least two clocks.

[Claim 54]: wherein a request to read data from one of the plurality of memory blocks is completed in at least three clocks.

[Claim 70]: during a second clock, issuing a stall signal to: the requester that issued an unsatisfied request, and the memory management circuits of respective memory blocks.

[Claim 78]: during a second clock, if the request is a request to read data from the requested memory block, further comprising: providing data retrieved from said one of the memory blocks onto a memory bus directed to the determined requester, wherein the memory block from which the retrieved data is stored is identified by a destination address retrieved from the determined requester while driving the first set of one or more requests onto the request bus during the first clock

[Claim 79]: during a fourth clock, further comprising latching the requested data retrieved from said one of the memory blocks internally to the determined requester.

[Claim 83]: the specific timing of the operations described in the claims.

Conclusion

60. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Anderson whose telephone number is (571) 272-4177. The examiner can normally be reached on Monday-Friday, 2nd Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew D. Anderson
Primary Examiner
Art Unit 2186